AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows in accordance with 37 C.F.R. § 1.121:

Pages 1 and 2, on the paragraph that begins with " in many types of data....."

In many types of data and voice networks such as xDSL, that employ fixed circuits to transport data, it is extremely important that a single timing source is referenced at each node in the network. Because over a period of time, a slight difference in system timing between nodes may result in buffer to overflow ~~or~~ underflow, where one of the devices on the network may transmit data in a slightly faster or slower ~~manner~~ rate than a receiving device would empty data from its buffer~~, therefore~~. Therefore, in an ATM network, it is necessary it is necessary to ensure that the clocks at each end node are synchronized and locked to the same timing reference. Time ~~compression~~ division multiplexing (TDM) is assumed as the end device, and that the timing reference for each TDM bus at the end of the network is obtained from a primary source outside the ATM network, and the timing reference is propagated across the network. The methods used to ensure that the timing source is carried accurately between nodes are, for example, adaptive clocking and synchronous residual time stamp (SRTS). In existing network timing recovery techniques such as synchronous residual time stamp (SRTS), the timing signal of a constant bit rate input service signal at the destination node of a synchronous ATM telecommunication network is recovered. At the source node, a free-running P-bit counter counts cycles in a common network clock. At the end of every RTS period formed by N service clock cycles, the current count of the P-bit counter, defined as the RTS, is transmitted in the ATM adaptation layer. Since the absolute number of network clock cycles likely to fall within an RTS period will fall within a range determined by N, the frequencies of the network and service clocks, and the tolerance of the service clock, P is chosen so that the 2.sup.P possible counts, rather than

representing the absolute number of network clock cycles an RTS period, provide sufficient information for unambiguously representing the number of network clock cycles within that predetermined range. At the destination node, a pulse signal is derived in which the periods are determined by the number of network clock cycles represented by the received RTSs. This pulse signal is then multiplied in frequency by N to recover the source node service clock. In the event that a "phase jump" occurs, where the frequency suddenly changes by a large amount, the telecommunications equipments connected to the multiplied clock output may function incorrectly, if a large frequency change is introduced on its clock inputs, thereby creating lack of synchronization between transmitter and receiver in a communication system.

Page 3, on the paragraph that begins with " In an additional embodiment....."

In an additional embodiment, the present invention further provides a configuration whereby the choice of external or internal 8kHz reference is controlled by software, and further ~~than~~ that said 8kHz reference is always used as the input to the PLL clock multiplier.

Pages 4 and 5, on the paragraph that begins with " Referring now to FIG. 1 ....."

Referring now to FIG. 1, there is shown a simplified block diagram illustrating one embodiment of a network timing recovery (NTR) method and apparatus 100 configured in accordance with the present invention. The purpose of the NTR device is to generate a multiplied bit rate clock phase locked to an 8kHz reference. The digital logic within the NTR implementation is clocked by a high speed bus clock, typically over 100 MHz. The method begins with the configuration and status registers 110, which are configured to allow the selection of various signal routing configurations and define various numerical constants. Status

information allows a software to determine if a digital phase locked loop DPLL 190 has achieved frequency lock. A ~~(1/N)~~ $(1/N_1)$ divider 140 operating on an external clock reference input 101. The value of ~~N~~ N_1 of divider 140 is selected by the configuration register 110 to be either 1, 256, 193 or 192 depending on whether the external clock frequency 101 is an 8kHz reference or a 2.048 MHz, ~~1.536 MHz or 1.544 MHz clock~~ 1.544 MHz or 1.536 MHz clock, respectively. The output of this divider is therefore always 8kHz. A ~~16 bit (1/Y)~~ $(1/Y_1)$ divider circuit 150 is clocked with a high-speed bus 180, and where the value of ~~Y~~ Y_1 is generated in a configuration register 110, and passed onto the ~~(1/Y)~~ $(1/Y_1)$ divider; in applications where an external 8kHz reference 101 is available which is the preferred operating mode, the DPLL 190 will be configured to phase lock to it, utilizing its limited bandwidth to reduce jitter on the output clock 195. However, in the more complex scenarios (adaptive clock recovery, synchronous residual timestamp, etc.) the burden is placed on the software to manipulate the ~~(1/Y)~~ $(1/Y_1)$ divider to generate a reference clock of a desired rate (either above or below the nominal 8kHz frequency) as deemed necessary to maintain synchronization with the far end equipment. The reference thus produced is sent to the DPLL 190, which filters out any jitter or non-continuities in its normal manner, thus, allowing very accurate specification of an 8kHz reference or one slightly higher or lower for adaptive clock recovery. As an example, if the ~~(1/Y)~~ $(1/Y_1)$ divider 150 is clocked with a high speed bus clock 180 running at 100 MHz then a value of ~~Y = 12500~~ $Y_1 = 12500$ gives an exact 8kHz output.

Pages 5 and 6, on the paragraph that begins with " In an another embodiment, and in reference to Figure 2....."

In another embodiment, and in reference to Figure 2, a digital phase locked loop (DPLL) 200 comprises a numerically controlled oscillator (NCO) 208, implemented as a ~~(Y/2N)~~ $(Y_2/2^{N_2})$ divider that receives a high-speed bus clock 210. The values of ~~N and Y~~ N_2 and Y_2 are chosen such that the center frequency of the divider is either 2.048 MHz, 1.544 MHz or 1.536 MHz (which are key telecoms standard bit rate clock frequencies). In a preferred implementation the value of N N_2 has been fixed for all frequencies to simplify the arithmetic logic, and the value of ~~Y~~ Y_2 is modified by the digital logic to produce the phase locking behavior of the DPLL. The greater the number of bits used to represent ~~N and Y~~ N_2 and Y_2 the better the accuracy of the centre frequency will be (but the digital arithmetic logic becomes increasingly complex and hence slower). The output of the numerically controlled oscillator (NCO) 208 is divided down with a ~~(1/N)~~ $(1/N_3)$ divider 212 to produce an 8kHz output reference 213. The value of ~~N~~ N_3 in the ~~(1/N)~~ $(1/N_3)$ divider 212 may be either 256, 193 or 192 depending on whether the numerically controlled oscillator (NCO) 208 clock output is 2.048 MHz, 1.544 MHz or 1.536 MHz respectively. The output of the ~~(1/N)~~ $(1/N_3)$ divider 212 is fed into a phase comparator 204 that compares a time delay between rising edges on this output reference signal 213 and an 8kHz input reference signal 202 to determine the sign and magnitude of any phase error between the two. The phase error is then passed onto a low pass filter 206 to ~~low pass~~ be filtered (i.e. divided by some constant value) and the result is fed into the numerically controlled oscillator (NCO) 208 as a correction factor to be used for the modification of its ~~Y~~ Y_2 value. In more detailed scenario, if the 8kHz reference edge occurs before the 8kHz numerically controlled oscillator (NCO) 208 edge then the numerically controlled oscillator (NCO) 208 frequency is determined to be too low so the numerically controlled oscillator (NCO) 208 ~~Y~~ Y_2 value is decreased by an amount proportional to the delta time between the two edges. Similarly, if the 8kHz reference

edge occurs after the 8kHz numerically controlled oscillator (NCO) 208 edge then the numerically controlled oscillator (NCO) 208 frequency is determined to be too high and the numerically controlled oscillator (NCO) 208 ~~Y~~ Y_2 value is reduced. The digital phase locked loop DPLL 200 is deemed to be "locked" to the reference when the magnitude of the phase error is small.

Page 7, on the paragraph that begins with " In applications where an external 8kHz ......"

In applications where an external 8kHz reference is available, the DPLL will be configured to phase lock to it, utilizing its limited bandwidth to reduce jitter on the output clock. This is the preferred operating mode. However, in the more complex scenarios (adaptive clock recovery, synchronous residual timestamp, etc.) the burden is placed on software to manipulate the ~~(1/Y)~~ ($1/Y_1$) divider to generate a reference clock of a desired rate (either above or below the nominal 8kHz frequency) as deemed necessary to maintain synchronization with the far end equipment. The reference thus produced is sent to the DPLL which will filter out any jitter or non-continuities in its normal manner. Using this arrangement has the advantage of guaranteeing that the multiplied clock output produced under software control will be constrained within the design parameters of standard telecommunications equipment.

Page 7, on the paragraph that begins with " One further capability ....."

One further capability that arises from this network timing recovery (NTR) method, is that it can be configured to take one frequency of multiplied reference as an input and generate a different (yet phase locked) multiplied output. For example, an output clock of 2.048 MHz

(telecommunications standard ~~"T1"~~ "E1" bit rate) can be generated from an external input clock of ~~1.544 MHz~~ 1.536 MHz (telecommunications standard ~~"E1"~~ "T1" bit rate) and vice versa.

Page 8, on the paragraph that begins with " Some TDM interface modes of operation ....."

Some TDM interface modes of operation may require higher frequencies than the standard 2.048 MHz, such as 16.384 MHz, 8.192 MHz and 4.096 MHz. The NTR block described above does not generate these clocks, and such applications will require an external clock synchronizer/generator. In these applications the NTR reference input to the NTR block will actually be the multiplied phase locked clock, so configuration options are also provided to bypass the NTR block altogether, or to divide this clock down to an 8 KHz reference. ~~The TDM block will generate the necessary select signals to achieve the required routing of its clock signals.~~

Page 8, on the paragraph that begins with " In another embodiment of the present invention, and in reference to Figure 3....."

In another embodiment of the present invention, and in reference to Figure 3, The method begins with receiving an external clock reference in step 305, the external clock value is divided by an integer ~~N~~ N_1 in step 315, in step 320 , a status register is configured to allow the selection of various signal routing configurations and define various numerical constants. The status register clock employs a high-speed bus clock, and it generates a ~~Y~~ Y_1 value in steps 325 and 330 respectively, the generated ~~Y~~ Y_1 value is passed onto 16 bit ~~(1/Y)~~ $(1/Y_1)$ divider circuit in step 335, the outputs of the ~~N-divider~~ N1-divider as well as the ~~Y-divider~~ Y_1-divider are passed

onto a an arithmetic logic unit in step 340, which in turn calculates a the external clock signal and passes it onto a digital phase-locked loop in step 345, which compares the a locally generated output reference signal to the input reference signal from the arithmetic logic unit in step 350. When the digital phase-locked loop locks on to the reference signal, the output is the desired result, otherwise the process goes back to step 345, until the desired result is achieved.

Page 11, on the paragraph that begins with " YVAL: The Y value....."

YVAL: The ~~Y~~ Y_1 value to use for the NTR ~~1/Y~~ $1 / Y_1$ divider.

Page 11, on the paragraph that begins with " YVAL: indicates....."

1: ~~'Other' taken to mean~~ 133 MHz.

Pages 12 and 13, on the paragraph that begins with " PLL_REFSRC: This flag....."

PLL_REFSRC: This flag determines whether the 8kHz reference source is taken from the incoming external NTR_CLK_IN signal or from the internal ~~1/Y~~ $1/Y_1$ divider. Its possible values are:

0: Use NTR_CLK_IN signal;

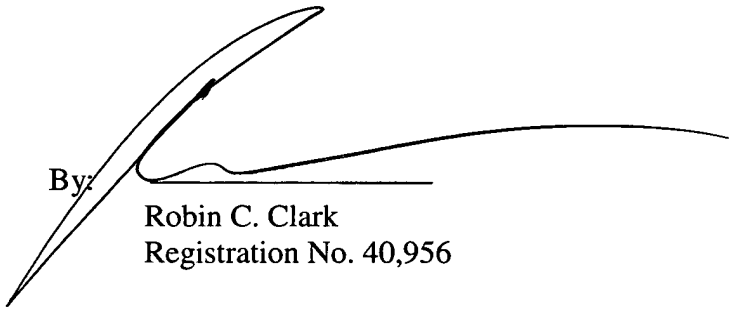
1: Use internal ~~1/Y~~ $1/Y_1$ divider.

REMARKS

Applicant believes that changes made to the specification do not add new matter, and are commensurate with the subject matter originally disclosed. More specifically, the changes made to the specification include typographical corrections, changes made to differentiate one element from other elements to further clarify the instant invention. A check in the amount of $234.00 is attached to cover the fee for additional claims. In the event of any variance between the amount enclosed and the fees determined by the U.S. Patent and Trademark Office, please charge or credit any such variance to the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

HUNTON & WILLIAMS LLP



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By: Robin C. Clark
Registration No. 40,956

Hunton & Williams LLP
Intellectual Property Department
1900 K Street, N.W.
Suite 1200
Washington, DC 20006-1109
(202) 955-1500 (telephone)
(202) 778-2201 (facsimile)